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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,696	11/06/2000	Joonbae Park	GCT-011	7786

7590 04/26/2004

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	9

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/705,696	PARK ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 3/1/04 in which claims 1-25 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-XXX are rejected under 35 U.S.C. 102(b) as being anticipated by Ward U.S. Patent No 5,703,292.

As per claims 1 and 7, Ward discloses a loop apparatus, comprising: a plurality of gain stages connected in series to amplify a signal having a voltage, wherein each gain stage increases the voltage of the signal, and includes an input port that receives the signal and an output port that transmits the resulting amplified signal (see figs. 3 elements 120, 122, 124, or 104, 107 or 130, 128, 140 and col.9, lines 35-67); a plurality of feedback loops (see fig.3 and abstract and col.2, lines 65-67 and col.3, lines 1-10, 53-67) that eliminate fading is considered as the claimed (cancel an undesired offset of the resulting amplified signal) wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that eliminates fading (cancels the

undesired offset) (see fig.3 and col.3, lines 1-10 and col.6, lines 35-42) of its corresponding gain stage.

As per claim 2, Ward does include a direct current offset voltage (see col.4, line 26 and col.9, lines 41-45).

As per claim 3, Ward inherently include a high-pass filter that filters the direct current offset voltage.

As per claim 4, Ward inherently includes a variable gain amplifier.

As per claim 5, Ward does include a CMOS is considered as the claimed (chip) (col.4, line 25), and each feedback loop includes a capacitor (fig.3 and col.3, line 51) mounted on the CMOS (chip).

As per claim 6, Ward inherently includes an analog radio frequency signal.

As per claim 8, Ward discloses a direct conversion receiver, comprising: an amplification unit that receives and amplifies a signal, wherein the amplification unit includes a plurality of gain stages connected in series to amplify the signal having a voltage, wherein each gain stage increases the voltage of the signal, and includes an input port that receives the signal and an output port that transmits the resulting amplified signal (see figs. 3 elements 120, 122, 124, or 104, 107 or 130, 128, 140 and col.9, lines 35-67); a plurality of feedback loops (see fig.3 and abstract and col.2, lines 65-67 and col.3, lines 1-10, 53-67) that eliminate fading is considered as the claimed (cancel an undesired offset of the resulting amplified signal) (see col.1, lines 19-20, 28-30, 46-47 and col.4, lines 44-47) wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that eliminates fading (cancels the undesired offset) (see fig.3 and

col.3, lines 1-10 and col.6, lines 35-42) of its corresponding gain stage; and a mixer (see fig. 14 element 648 or 626 and col.22, lines 41-67 and col.23, lines 1-10) that demodulates the amplified signal by mixing the amplified signal with a local oscillation signal to form a demodulated base band signal.

As per claims 9, 19, 23, Ward inherently includes an analog-to digital converter that converts the demodulated base band signal to a digital data stream.

As per claim 10, Ward inherently includes a channel selection filter that removes an out-of-band signal from the demodulated base band signal.

As per claim 11, Ward does include a direct current offset voltage (see fig.3 and col.4, line 26), and each feedback loop includes eliminate fading is considered as the claimed (cancel an undesired offset of the resulting amplified signal) (see fig.3 and col.3, lines 1-10 and col.6, lines 35-42) direct current offset canceling unit for rejecting the direct current offset voltage accumulated by its corresponding gain stage.

As per claim 12, Ward inherently includes a high-pass filter that filters the direct current offset voltage.

As per claim 13, Ward inherently includes a variable gain amplifier.

As per claim 14, Ward does include a CMOS is considered as the claimed (chip) (col.4, line 25), and each feedback loop includes a capacitor (fig.3 and col.3, line 51) mounted on the CMOS (chip).

As per claims 15, 17, 21 and 25,Ward inherently includes an analog radio frequency signal.

As per claim 16, Ward inherently includes plurality of clock signals to generate the local oscillator signal, wherein each of the clock signals has a frequency less than the local oscillator signal.

As per claims 18, 22 Ward does include a mixer (see fig. 14 element 648 or 626 and col.22, lines 41-67 and col.23, lines 1-10) that demodulates the amplified signal by mixing the amplified signal with a local oscillation signal to form a demodulated base band signal.

As per claims 20, 24 Ward inherently includes a single amplification unit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ward U.S. Patent No 5,608,351 teaches electronics for coriolis force

Goldberg U.S. Patent No 5,553,151 teaches an electro acoustic speech.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 703 308-9573. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 703 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

4/22/04